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He has been a consultant to a large number of electronic firms. During 1968–1969, he was Liaison Scientist for the U.S. Office of Naval Research in London. He is a member of Tau Beta Pi and recipient of the 1976 Morris N. Liebmann Memorial Award of the IEEE "for contributions to the development of acoustic surface wave devices," and the 1981 Achievement Award of the IEEE group on Sonics and Ultrasonics "for many contributions, through research and education, to ultrasonics technology."

Graphic Design of Matching and Interstage Lossy Networks for Microwave Transistor Amplifier

JUAN CARLOS VILLAR AND FÉLIX PÉREZ

Abstract—**A graphical design method for lossless and lossy gain-compensating networks is presented, and the advantages of the use of this technique in the construction of microwave transistor amplifiers are discussed. The method is based on the use of a set of constant $|S_{ji}|$ circles plotted on the Smith Chart, and is easily automated on a personal computer. Two applications are presented: a two-stage amplifier with 20 dB in the 100–1100-MHz band and an ultra-broad-band lossy matched amplifier stage with 4 dB in the dc–16-GHz band.**

I. Introduction

IN ORDER TO DESIGN wide-band microwave amplifiers, it is necessary to compensate for transistor gain roll-off with frequency. Usually this compensation is achieved by lossless coupling networks which reflect unwanted available power for low frequencies. Several analytical design techniques for lossless equalizers have been reported [1], [2], like the well-known constant gain circles graphic method [3]. However, these techniques are not satisfactory in many cases, and lossy equalizers must be employed to obtain a flat gain response, especially in the design of ultra-wide-band amplifiers.

Several design methods for lossy equalizers have been reported. However, particular networks have been proposed by these authors, yet their methods cannot be applied to all configurations [4], [5]. This paper presents a new graphic design method with a wider field of application, which allows us to calculate matching and interstage lossless and lossy networks with any configuration, and is an excellent first step in the design of wide-band amplifier modules. The technique is similar to the constant gain circles method, and is based on the use of a set of curves of constant $|S_{ji}|$, plotted on the Smith Chart, that leads in a simple way to the structure of the networks in order to obtain gain equalization and matching in the transistor ports. Additional advantages of this procedure are the

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characterization of the devices by their S parameters and the easy way that can be automated on a personal computer.

The basic theory and the construction rules of constant $|S_{ji}|$ circles are discussed first. Then, we describe the application of the method with two examples: a multistage bipolar amplifier in the 100–1100-MHz frequency range and an ultra-broad-band matched FET amplifier covering the dc–16-GHz frequency range.

II. Basic Theory: Constant Gain Circles

Consider the circuits shown in Fig. 1. If the two-port networks are characterized, in each case, by their Z or Y parameters, the S parameters of the overall circuits are given by the following expressions:

$$S_{ji}^T = \frac{A + BZ_E}{C + DZ_E} \tag{1}$$

$$S_{ji}^T = \frac{A' + B'Y_E}{C' + D'Y_E} \tag{2}$$

where A, B, C, and D depend only on the $[Z]$ and $[Z']$ parameters and on the $[Y]$ and $[Y']$ parameters, respectively.

Equation (1) represents a bilinear transformation between the complex planes S_{ji}^T and Z_E. The constant $|S_{ji}^T|$ circles are transformed into other circles on the Z_E plane. Moreover, if a new bilinear transformation is considered

$$\alpha = \frac{Z_E - Z_0}{Z_E + Z_0} \tag{3}$$

we may conclude that the constant $|S_{ji}^T|$ circles are transformed into other new circles on the Smith Chart.

For the circuit shown in Fig. 1(b), the constant $|S_{ji}^T|$ geometrical loci on the admittance Smith Chart will also be circles.

A. Interstage Networks Design

In the design of wide-band amplifier modules, configurations like those shown in Fig. 1 are generally used. The two-port networks represent the active devices and the interstage networks equalize the gain roll-off with frequency. The constant $|S_{21}^T|$ circles on the Smith Chart are a family of circles (see Appendix I) whose centers and radii are

$$\alpha_0 e^{j\theta_0} = \frac{2(1+\gamma_c^*)}{r^2 - |1+\gamma_c|^2} + 1 \tag{4}$$

$$R = \frac{2r}{|r^2 - |1+\gamma_c|^2|} \tag{5}$$

where

$$\gamma_c = \frac{\gamma_{12}\gamma_{21}}{1+\gamma_{11}} + \frac{\gamma_{12}'\gamma_{21}'}{1+\gamma_{22}'} - \gamma_{11}' - \gamma_{22} \tag{6}$$

$$r = \frac{2}{|S_{21}^T|}\left|\frac{\gamma_{21}\gamma_{21}'}{(1+\gamma_{11})(1+\gamma_{22}')}\right| \tag{7}$$

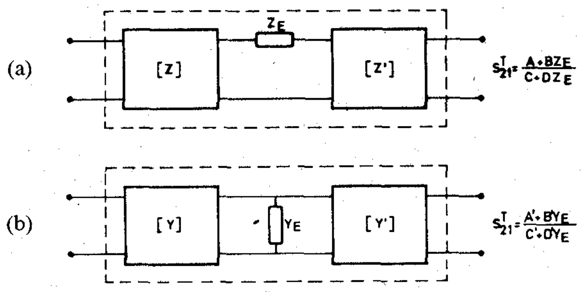

Fig. 1. Basic structures for interstage networks design.

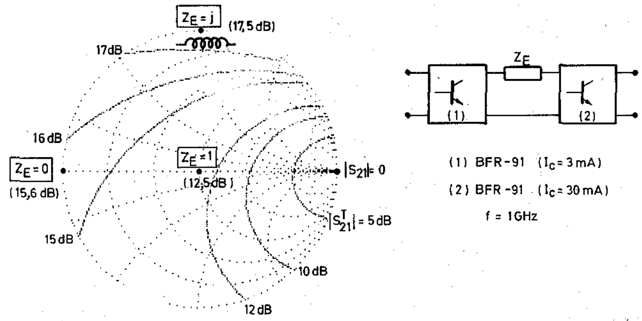

Fig. 2 Constant $|S_{21}|$ circles on impedance Smith Chart ($Z_0 = 50\ \Omega$).

and the circles are on the impedance or admittance Smith Chart and γ_{ij} are the normalized Z or Y parameters, depending on the configuration used (Fig. 1(a) or (b)).

In Fig. 2, we have represented the constant $|S_{21}|$ circles for a particular case. If both transistors are connected directly ($Z_E = 0$) the circuit gain is 15.6 dB, but if we introduce an impedance Z_E, the gain is determined by the circle that passes through that impedance. For a passive impedance Z_E, the graph indicates that the maximum gain is obtained with an inductor $L = 7.96$ nH($Z_E = +j1$).

In a broad-band design, we can plot the circles of desired value $|S_{21}^T|$ for several frequencies in the band, and then synthesize the interstage networks whose impedance Z_E or admittance Y_E falls on the respective circle at each frequency.

B. Matching and Equalization Networks Design

Consider now the circuit shown in Fig. 3. We can use the constant $|S_{21}|$ and constant $|S_{ii}|$ circles to control both gain and matching.

The centers and radii of these circles are (see Appendix II)

$$\alpha_0 e^{j\theta_0} = \frac{2(1+\gamma_c^*)}{r^2 - |1+\gamma_c|^2} + 1 \tag{8}$$

$$R = \frac{2r}{|r^2 - |1+\gamma_c|^2|} \tag{9}$$

where, for constant $|S_{21}|$

$$\gamma_c = \frac{\gamma_{12}\gamma_{21}}{1+\gamma_{jj}} - 1 - \gamma_{ii} \tag{10}$$

$$r = 2|\gamma_{21}|/|1+\gamma_{jj}||S_{21}| \tag{11}$$

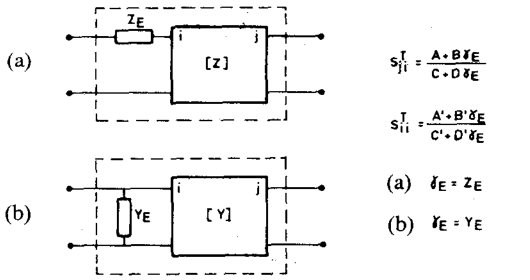

Fig. 3 Basic structures for matching and equalization networks design.

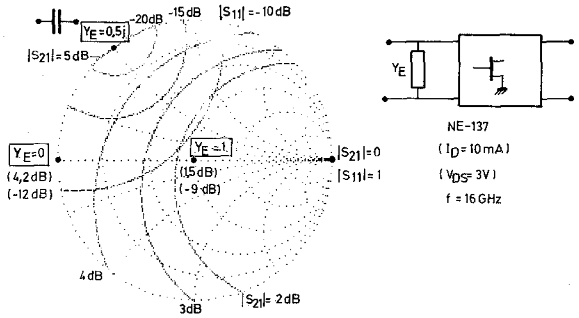

Fig. 4 Constant $|S_{21}|$ and $|S_{11}|$ circles on admittance Smith Chart ($Z_0 = 50\ \Omega$).

and for constant $|S_{ii}|$

$$\gamma_c = \frac{2}{1-|S_{ii}|^2} + \frac{\gamma_{12}\gamma_{21}}{1+\gamma_{jj}} - 1 - \gamma_{ii} \tag{12}$$

$$r = 2|S_{ii}|/(1-|S_{ii}|^2). \tag{13}$$

γ_{ij} are the Z or Y parameters and the circles must be plotted on impedance or admittance Smith Chart for series or parallel configuration, respectively.

In Fig. 4, we present the circles at 16 GHz for a NE-137 (Nippon Electric Co.) transistor. If there is no admittance $(Y_E = 0)|S_{21}| = 4.2$ dB and $|S_{11}| = -12$ dB, and perfect matching can be achieved by a capacitor of $C = 0.1$ pF in parallel with the port of the transistor and the overall gain increases to 5 dB.

In broad-band design, we synthesize the matching and equalization network by plotting the $|S_{21}|$ and $|S_{ii}|$ circles for several frequencies in the band, and by determining the admittance Y_E or impedance Z_E in order to obtain flat gain and good matching in the full band.

In the next sections, we present two examples of the use of these techniques. In both cases, transistors are characterized by the S parameters supplied by the manufacturer.

III. Examples

A. Amplifier Stage in the 100–1100-MHz Frequency Range

First we shall apply this technique to the design of an amplifier stage with 20-dB gain from 0.1–1.1 GHz. Two BFR91 (Siemens) bipolar transistors with $f_T = 4.5$ GHz were used.

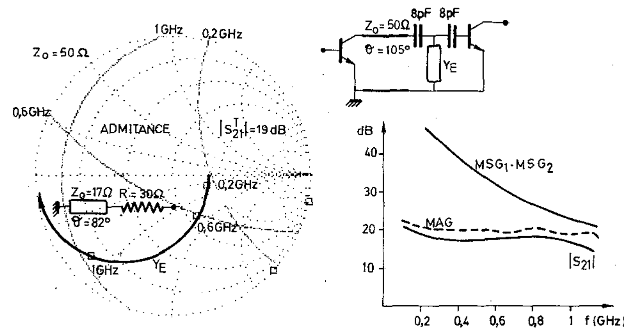

Fig. 5 Graphic design of interstage networks.

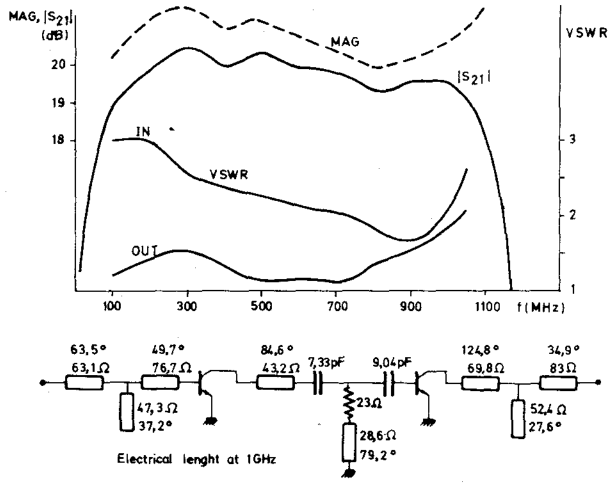

Fig. 6 Amplifier module and its characteristics.

The amplifier module consists of two stages coupled by a lossy interstage network to equalize the gain of the devices. The first stage is baised for low noise ($I_c = 3$ mA, $V_{cE} = 8$ V) and the second one for high gain ($I_c = 30$ mA, $V_{cE} = 8$ V).

In Fig. 2, we have plotted the constant $|S_{21}|$ circles at $f = 1$ GHz on the impedance Smith Chart. A graphical inspection shows that is impossible to obtain a 20-dB gain using series impedances with positive real parts. If constant $|S_{21}|$ circles are plotted on the admittance Smith Chart, with equalization accomplished with a parallel network, the results are similar. Therefore, as the product of the maximum stable gain (MSG) of both devices at this frequency is 23 dB, it is clearly seen that a simple series impedance or parallel admittance cannot match both transistors. In fact, we have proven that with this configuration it is better to design first a simple matching network at the highest frequency of interest, and then "open" it at different points, plotting the constant $|S_{21}|$ circles, until the most adequate position to introduce the series or parallel equalization network is found.

Again in the design, a possible matching network at 1 GHz consists of a section of line ($Z_0 = 50\ \Omega, \theta = 105°$ (1 GHz)) is series with a capacitor of 4 pF. In Fig. 5, the circles for $|S_{21}| = 19$ dB, with a parallel equalization network connected at an inner point of the matching network are represented. By trial and error on the Smith Chart, we

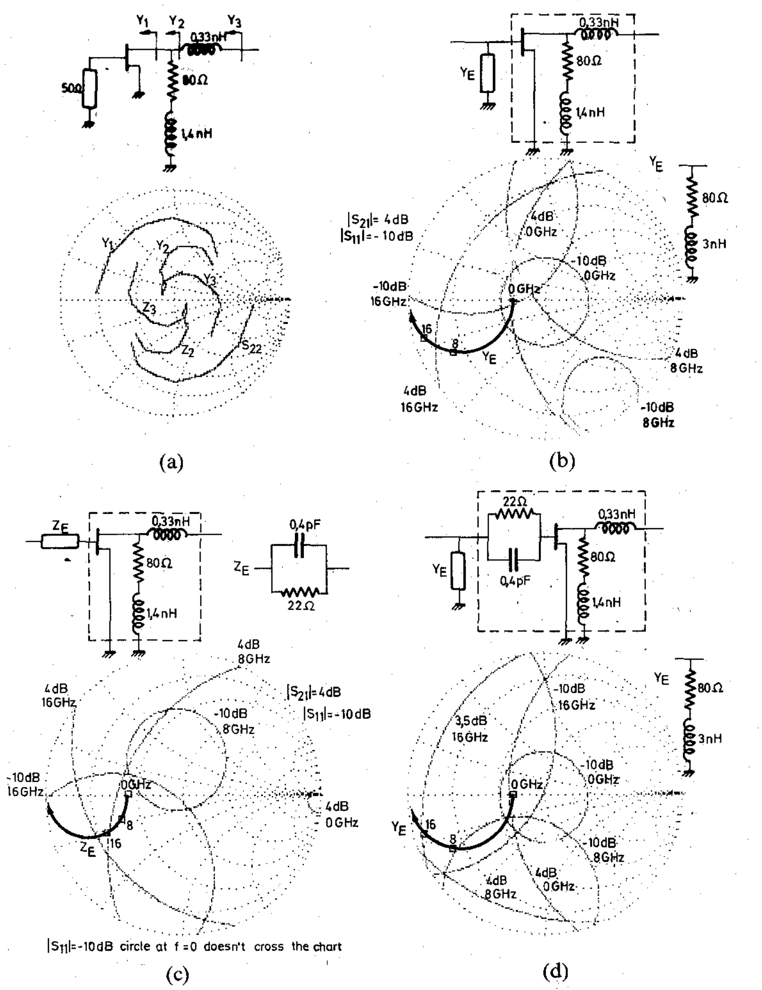

Fig. 7 Lossy match amplifier design.

finally choose a series resistance-shunt stub network ($R = 30\ \Omega, Z_0 = 17\ \Omega, \theta = 82°$(1 GHz)) which equalizes the response of the circuit. In the same figure, the resultant circuit MAG and the product of the devices' MSG's are compared (we cannot define the MAG of the first transistor because it is conditionally stable at this frequency range). It is evident that the interstage network provides stability and equalization to the devices.

Finally, we proceed to the design of the input and output matching networks. Some graphic work on the Smith Chart, followed by computer optimization aiming a flat gain of 20 dB, leads to the amplifier stage whose schematic is indicated in Fig. 6, together with its theoretical response. The amplifier gain is 20 ± 0.6 dB in the band, though the input VSWR is high because it has not been taken into account in the optimization procedure. This power reflection may be compensated by means of balanced configurations, isolators, etc., or, as the circuit has a flat MAG, by designing more sophisticated matching networks that provide a good broad-band matching of the amplifier module.

B. Ultra-Broad-Band (DC–16-GHz) Transistor Amplifier Stage

Ultra-broad-band matched amplifiers with flat gain responses and low VSWR's over a frequency range of several octaves have extensive application areas, including optical communication and data transmission systems, military electronics (ECM), and CATV applications. To achieve these characteristics, three different configurations have been proposed: feedback, distributed, and lossy matched amplifier [6]–[9].

We shall now describe the application of the proposed method to the design of an ultra-broad-band lossy matched amplifier stage with a 4-dB gain covering the dc–16-GHz frequency range. We use a commercially available transistor NE 137. The low gain is due to the need for low frequency matching and to the low transconductance of MESFET devices [10].

In the design of the amplifier stage, we must first match one of the ports, and then, with the help of the constant $|S_{ji}|$ circles, determine the network that provides good matching in the other port and equalizes the response in the whole band.

In this case, it is easy to find the output matching network as shown in Fig. 7(a). In Fig. 7(b), we present the constant $|S_{21}|$ and $|S_{11}|$ circles for three frequencies in the band.

The set of curves points to the fact that in the low-frequency range only a LR series network in shunt connection allows us to match the input port and to equalize the stage gain, while for high frequencies, the adequate net-

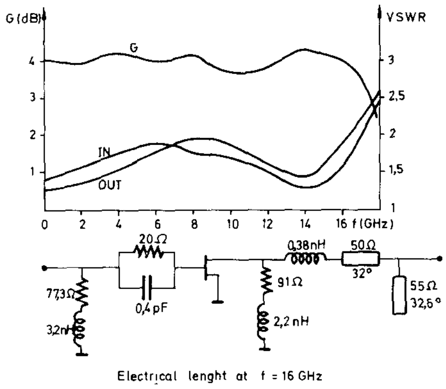

Fig. 8 DC–16-GHz amplifier stage.

work is a *RC* parallel network in series connection (Fig. 7(c)). In fact, the solution is to use both circuits, as shown in Fig. 7(d).

Finally, the complete circuit has been optimized by computer resulting in the final configuration and results shown in Fig. 8. An additional network has been introduced in the output port to get better matching in high frequencies. As it can be seen, the amplifier gain is 4 ± 0.3 dB and the VSWR's are lower than 2 between dc and 16 GHz. (Obviously, the low cutoff frequency will be determined by the coupling capacitors.)

IV. Conclusion

A graphical procedure for the design of lossy equalized transistor amplifiers has been described. We have shown how easy it is to find the appropriate equalization network plotting the constant $|S_{ji}|$ circles on the Smith Chart.

The graphical method has then been applied to the design of a 0.1–1.1-GHz two-stage amplifier with 20-dB gain, using a BFR91 bipolar transistor with $f_t = 4.5$ GHz. Coupling the active devices with a very simple lossy network, a flat gain of more than one decade bandwidth, has been obtained.

As a second application of this method, an ultra-wideband MESFET amplifier stage has been designed. Using a NE137 MESFET chip and lossy matching networks, we have designed an amplifier stage with 4-dB gain in the dc–16-GHz frequency band and low reflection parameters ($|S_{11}| < -11$ dB, $|S_{22}| < -10$ dB in the full band).

Finally, we must remark that this procedure is easily automated in personal computers, and is therefore an important tool for the design of equalized microwave amplifiers.

Appendix I

If the total S parameters of any circuit can be expressed as

$$S = \frac{AH + B}{CH + D} \tag{A1}$$

the $|S| = M$ circles are transformed into other circles in the H plane whose centers and radii can be easily calculated as follows.

In polar coordinates, $H = \rho e^{j\theta}$ and substituting H we may write

$$|S|^2 = S \cdot S^* = \frac{A\rho e^{j\theta} + B}{C\rho e^{j\theta} + D} \cdot \frac{A^*\rho e^{-j\theta} + B^*}{C^*\rho e^{-j\theta} + D^*} = M^2. \tag{A2}$$

After doing some algebra, we can transform (A2) into the following expression:

$$\begin{aligned} &\rho^2\left(|A|^2 - M^2|C|^2\right) + \rho\left(AB^*e^{j\theta}\right. \\ &\quad \left.+ BA^*e^{-j\theta} - M^2CD^*e^{j\theta} - M^2C^*De^{-j\theta}\right) \\ &\quad + |B|^2 - m^2|D|^2 = 0 \end{aligned} \tag{A3}$$

which represents a family of circles whose centers and radii are given by

$$|H - \gamma_c|^2 = r^2 \tag{A4}$$

$$\gamma_c = \frac{M^2C^*D - BA^*}{|A|^2 - M^2|C|^2} \tag{A5}$$

$$r = \left(|\gamma_c|^2 - \frac{|B|^2 - M^2|D|^2}{|A|^2 - M^2|C|^2}\right)^{1/2}. \tag{A6}$$

If we express the parameter H as a function of a reflection coefficient

$$H = \frac{1 + \Gamma}{1 - \Gamma} \tag{A7}$$

the family of circles (A4) may be rewritten as

$$r^2 = \left|\frac{1 + \Gamma}{1 - \Gamma} - \gamma_c\right|^2 ; \; r|1 - \Gamma|^2 = |\Gamma(1 + \gamma_c) + 1 - \gamma_c|^2. \tag{A8}$$

After some algebra, we can transform (A8) into a more familiar expression

$$\left(\mathrm{Re}(\Gamma) - \frac{r^2 + 1 - |\gamma_c|^2}{r^2 - |1 + \gamma_c|^2}\right)^2 + \left(\mathrm{Im}(\Gamma) + \frac{2I_m(\gamma_c)}{(r^2 - |1 + \gamma_c|^2)}\right)^2 = \frac{4r^2}{\left(r^2 - |1 + \gamma_c|^2\right)^2}$$

which represents a family of circles on the Smith Chart with centers and radii

$$\rho_0^{e^{j\theta}} = \frac{2(1 + \gamma_c^*)}{r^2 - |1 + \gamma_c|^2} + 1 \tag{A10}$$

$$R = \frac{2r}{|r^2 - |1 + \gamma_c|^2|}. \tag{A11}$$

If we analyze the circuits shown in Fig. 1 using the equivalent circuits of the two-port networks, and we apply

(A5) and (A6)

—parameter S_{21}—

$$A = 0 \quad B = 2\gamma_{21}\gamma'_{21}/(1+\gamma_{11})(1+\gamma'_{22})$$

$$C = 1 \quad D = \gamma'_{11} + \gamma_{22} - \gamma'_{12}\gamma'_{21}/(1+\gamma'_{22}) - \gamma_{12}\gamma_{21}/(1+\gamma_{11})$$

$$\gamma_c = \frac{\gamma_{12}\gamma_{21}}{1+\gamma_{11}} + \frac{\gamma'_{12}\gamma'_{21}}{1+\gamma'_{22}} - \gamma'_{11} - \gamma_{22} \tag{A12}$$

$$r = \frac{2|\gamma_{21}\gamma'_{21}|}{|S_{21}||1+\gamma_{11}||1+\gamma'_{22}|} \tag{A13}$$

—parameter S_{11}—

$$A = 1 - \gamma_{11} \qquad B = \gamma_{12}\gamma_{21} - \gamma'_{12}\gamma'_{21}/(1-\gamma_{11})(1+\gamma'_{22}) + (1-\gamma_{11})(\gamma'_{11}+\gamma_{22})$$

$$C = 1 + \gamma_{11} \qquad D = -\gamma_{12}\gamma_{21} - \gamma'_{12}\gamma'_{21}/(1+\gamma_{11})(1+\gamma'_{22}) + (1+\gamma_{11})(\gamma'_{11}+\gamma_{22}).$$

Parameter S_{22} has the same expressions changing $\gamma_{ij} = \gamma'_{ji}$, and $\gamma'_{ij} = \gamma_{ji} \cdot \gamma_{ij}$ are the normalized Z or Y parameters, depending on the configuration used (Fig. 1(a) or (b)).

Appendix II

Let us consider the circuits shown in Fig. 3. Knowing that $\gamma_{ii}^T = \gamma_{ii} + \gamma_E$ and applying (A5) and (A6)

—parameter S_{21}—

$$A = 0 \quad B = -2\gamma_{21}/(1+\gamma_{jj})$$

$$C = 1 \quad D = 1 + \gamma_{ii} - \gamma_{12}\gamma_{21}/(1+\gamma_{jj})$$

$$\gamma_c = \frac{\gamma_{12}\gamma_{21}}{1+\gamma_{jj}} - 1 - \gamma_{ii} \tag{A14}$$

$$r = \frac{2|\gamma_{21}|}{|S_{21}||1+\gamma_{jj}|} \tag{A15}$$

—parameter S_{ii}—

$$A = -1 \quad B = 1 - \gamma_{ii} + \gamma_{12}\gamma_{21}/(1+\gamma_{jj})$$

$$C = 1 \quad D = 1 + \gamma_{ii} - \gamma_{12}\gamma_{21}/(1+\gamma_{jj})$$

$$\gamma_c = \frac{\gamma_{12}\gamma_{21}}{1+\gamma_{jj}} - 1 - \gamma_{ii} + \frac{2}{1-|S_{ii}|^2} \tag{A16}$$

$$r = \frac{2|S_{ii}|}{1-|S_{ii}|^2}. \tag{A17}$$

The centers and radii of the circles on the Smith Chart will be calculated using expressions (A10) and (A11).

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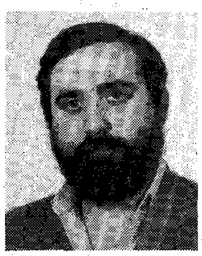

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